

● PRINTER RUSH ●
(PTO ASSISTANCE)

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<input type="checkbox"/> 1449		<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS		<input type="checkbox"/> Foreign Priority
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<input type="checkbox"/> IIFW		<input type="checkbox"/> Fees
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<input type="checkbox"/> DRW		
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<input type="checkbox"/> 312		
<input checked="" type="checkbox"/> SPEC	<u>12-29-05</u>	

[RUSH] MESSAGE: Lines 17, 21 and 25 of pg. 1 of specification
are missing serial nos. Only attorney docket nos. are
listed.

Please resolve.

Thank you.

[XRUSH] RESPONSE:

DONE

INITIALS: [Signature]

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REV 10/04

A CONFIGURABLE ALL-DIGITAL COHERENT DEMODULATOR SYSTEM
FOR SPREAD SPECTRUM APPLICATIONS

5 CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to the provisional patent application with the following Serial Number: 60/173,633, filed on December 30, 1999.

Related applications which are incorporated herein by reference, are:

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A CONFIGURABLE MULTIMODE DESPREADER FOR SPREAD SPECTRUM APPLICATIONS

Serial No. ⁰⁹⁷⁵¹⁷⁸⁵ ~~To Be Assigned~~, Attorney Docket No. 9824-0036-999 *filed 12/29/2000*

15 APPARATUS AND METHOD FOR CALCULATING AND IMPLEMENTING A FIBONACCI MASK FOR A CODE GENERATOR

Serial No. ⁰⁹⁷⁵¹⁷⁷⁶ ~~To Be Assigned~~, Attorney Docket No. 9824-0032-999 *filed 12/29/2000*

A FAST INITIAL ACQUISITION & SEARCH DEVICE FOR A SPREAD SPECTRUM

20 COMMUNICATION SYSTEM

Serial No. ⁰⁹⁷⁵¹⁷⁷⁷ ~~To Be Assigned~~, Attorney Docket No. 9824-0033-999 *filed 12/29/2000*

A CONFIGURABLE CODE GENERATOR SYSTEM FOR SPREAD SPECTRUM APPLICATIONS

25 Serial No. ⁰⁹⁷⁵¹⁷⁸² ~~To Be Assigned~~, Attorney Docket No. 9824-029-999 *filed 12/29/2000*

METHOD AND APPARATUS TO SUPPORT MULTI STANDARD, MULTI SERVICE BASE-STATIONS FOR WIRELESS VOICE AND DATA NETWORKS


Serial No. ⁰⁹⁷⁵²⁰⁵⁰ ~~To Be Assigned~~, Attorney Docket No. 9824-0035-999 *filed 12/29/2000*

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IMPROVED APPARATUS AND METHOD FOR MULTI-THREADED SIGNAL PROCESSING

Serial No. 09/492,634, filed on January 27, 2000

35 Except for application Serial No. 09/492,634, all of the above applications are filed simultaneously herewith.

 provided in the above-referenced co-pending US patent application serial number 09751785, entitled "A CONFIGURABLE MULTIMODE DESPREADER FOR SPREAD SPECTRUM APPLICATIONS" (attorney docket number 9824-0036-999).

5 Referring now to Figure 3, a block diagram of a configurable traffic channel demodulator (TCD) is shown, in accordance with one embodiment of the present invention. TCD 114 of Figure 3 provides an exemplary traffic channel demodulator for application in configurable demodulator kernels 174-1 and 174-2 of Figures 1C and 1D, respectively. TCD 114 receives code demodulated samples, on lines 180 and 182, from ELCD 112 and
10 performs sample energy accumulation operations and multiple phase shift keying (MPSK) operations to produce a demodulated output data sample, on line 184, which has not been corrected for phase errors. The operation of TCD 114 is described in more detail in a subsequent flowchart.

15 TCD 114 essentially has two parallel branches, one for operations to obtain a real sample, and one for operations to obtain a quadrature-phase sample. In particular, TCD 114 includes a first multiply-logic device 302 on one branch that is coupled to input line 180, whose source is ELCD 112 of Figure 2. Similarly, TCD 114 includes a second multiply-logic device 304 on another branch that is coupled to input line 182, whose source is ELCD
20 112 of Figure 2. Both multiply logic devices 302 and 304 have inputs to receive a traffic code sequence 164a. TCD 114 can demodulate any traffic channel code sequence, given the appropriate configuration instructions, e.g. TCD code configuration input 164 of Figure 1 that specifies the TCD code sequence input 164a. In the present embodiment, traffic code sequence input 164a is a W_d that is based on a short Walsh code. However, traffic code
25 sequence input 164a can be based on another code sequence in another embodiment.

A first sum and dump, or accumulator, circuit 306 is coupled to multiply-logic device 302, while a second sum and dump, or accumulator, circuit 308 is coupled to multiply-logic device 304. Both sum and dump circuits 306 and 308 have inputs to receive
30 an observation length 154 that establishes the number of sum operations required before a dump operation is performed on an in-phase portion and a quadrature-phase portion of the sum. Thus, sum and dump circuits 306 and 308 have a configurable accumulate, or integration, length. In this manner, the present invention allows TCD 114 to be configured for a given user, application, and/or performance level. First accumulator 306 and the
35 second accumulator 308 each have separate add-logic devices for adding the in-phase